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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/922,423	08/03/2001	Varadarajan Srinivasan	N1-P102	7436

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EXAMINER	
CHUNG, PHUNG M	
ART UNIT	**PAPER NUMBER**
2133	8

DATE MAILED: 07/02/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/922,423	SRINIVASAN ET AL	
	Examiner	Art Unit	
	Phung My Chung	2133	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☐ Responsive to communication(s) filed on _____.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-67* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-67* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *17 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *2, 3, 6*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

1. Claim 22 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

As per claim 22, line 1, "the second circuit" does not have a clear antecedent basis;

Line 3, "the first circuit" does not have a clear antecedent basis.

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 21-26, 41-45 and 57-63 are rejected under 35 U.S.C. 102(b) as being anticipated by Levitan (5,796,758).

As per claims 21 and 26, Levitan discloses a content addressable memory (CAM) device, comprising:

A CAM array including a plurality of rows of CAM cells and a plurality of validity storage cells; and

An error detection circuit coupled to the CAM array to receive a data word from a selected one of the rows of CAM cells and to receive a corresponding validity value from one of the validity storage cells. (See Fig. 1, col. 2, line 66 to col. 3, line 32).

As per claim 22-23, Levitan further discloses a first circuit to determine if the data word includes an error; and

A second circuit being configured to output an error signal or a valid value dependent upon the results of the first circuit. (See col. 3, lines 16-32).

As per claim 24, Levitan further discloses the first circuit includes a parity generation circuit to generate a parity value based on the CAM word. (See col. 3, line 16-35).

As per claim 25, Levitan further discloses the first circuit includes a compare circuit to compare the parity value generated by the parity generation circuit with a parity value that corresponding to the selected one of the rows of CAM cells. (See col. 3, lines 25-27).

As per claims 41-45, these claims are also rejected under the same rationale as set forth in claims 21-26.

As per claims 57-63, these claims are also rejected under the same rationale as set forth in claims 21-26.

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

This application currently names joint inventors. In considering patentability of the claims under 35 U.S.C. 103(a), the examiner presumes that the subject matter of the various claims was commonly owned at the time any inventions covered therein were made absent any evidence to the contrary. Applicant is advised of the obligation under 37 CFR 1.56 to point out the inventor and invention dates of each claim that was

not commonly owned at the time a later invention was made in order for the examiner to consider the applicability of 35 U.S.C. 103(c) and potential 35 U.S.C. 102(e), (f) or (g) prior art under 35 U.S.C. 103(a).

5. Claims 1-13, 16-20, 27-30, 32-40, 46-48 and 64-67 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nataraj et al (6,154,384) in view of Levitan (5,796,758).

As per claims 1, 2, 4-7, 9 and 10 , Nataraj et al disclose the invention substantially as claimed, comprising: a CAM array including a plurality of CAM cells, a plurality of bit lines and a plurality of comparand lines being adapted to provide as part of a compare operation, a comparand value for comparison with data words stored in the CAM cells. (See col. 2, lines 30-44). Nataraj et al do not specifically disclose an error detection circuit to determine whether the selected data word includes an error. However, Levitan disclose an error detection circuit to determine whether the selected data word includes an error. (See col. 3, lines 16-25). Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the error detection circuit of Levitan into the CAM array of Nataraj et al so that a self-checking content addressable memory utilize a minimum amount of logic to detect an error condition.

As per claims 3-7, the teaching of Nataraj et al and Levitan have been discussed above. Levitan further discloses: wherein the CAM array further includes storage cells to store a plurality of validity values, each validity value indicating whether a respective row of CAM coees contains a valid data word, the circuitry to assert the error signal

being coupled to receive one of the validity values that corresponds to the selected data word and including circuitry to prevent assertion of the error signal if the one of the validity values indicates that the selected data word is not a valid data word. (Col. 1, lines 15-28 and col. 2, lines 7-9).

As per claim 8, the teaching of Nataraj et al and Levitan have been discussed above. Levitan further disclose wherein the error detection circuit includes circuitry to determine whether the selected data word has a parity error. (See col. 3, lines 15-32).

As per claim 11, Nataraj et al further disclose: wherein each of the plurality of CAM cells is a ternary CAM cell. (Col. 1, lines 5-6 and col. 2, lines 30-31).

As per claims 12 and 13, Nataraj et al further disclose wherein the selected data word is a local mask value and is a CAM word. (Col. 1, lines 39-41).

As per claim 16, this claim is also rejected under the same rationale as set forth in claim 1.

As per claim 17, this claim is also rejected under the same rationale as set forth in claim 8.

As per claim 18-20, these claims are also rejected under the same rationale as set forth in claims 11-13.

As per claims 27-30, 32-34. these claims are also rejected under the same rationale as set forth in claims 1-13.

As per claims 35-40, and 46-48, these method claims are also rejected under the same rationale as set forth in system claims 1-13.

As per claims 64-67, these claims are also rejected under the same rationale as set forth in claims 1-13.

6. Claims 14-15 and 31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nataraj et al (6,154,384) and Levitan (5,796,758) as applied to claim 1 above, and further in view of ("Error Correction with Hamming Codes", PP. 1-2 downloaded June 22, 2001 from URL http://www.rad.com/networks/1994/err_con/hamming.htm).

As per claims 14-15, the teaching of Nataraj et al and Levitan have been discussed above. They do not disclose an error correction circuit for correcting error in the selected data word to generate a correct data word. However, "the Error Correction with Hamming Codes" does disclose correction of the selected data word. Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the error correction of the selected data word as taught by "the Error Correction with Hamming codes" into the invention of Nataraj et al and Levitan so that error can be corrected as a lower cost. (See pg.1, lines 5-7).

As per claims 31, this claim is also rejected under the same rationale as set forth in claim 14.

7. Claims 49-56 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nataraj et al (6,154,384) and Levitan (5,796,758) as applied to claims 1-13 above, and further in view of the admitted prior art.

As per claime 49 and 51-56, the teaching of Nataraj et al and Levitan had been discussed above. They do not disclose a processor is coupled to a plurality of signal

lines to a CAM device. However, the admitted prior art discloses that CAM device which is known to store parity information for error detection purposes and are often used in network switching and is connected to a host device. Therefore, it would have been obvious to a person of ordinary skill in the art, at the time the invention was made, to incorporate the processor that connected to CAM device in a network of the admitted prior art into the invention of Hataraj et al and Levitan so that the CAM device can signal the processor when error is detected. (See pgs. 1-2).

As per claim 50, the teaching of Nataraj et al, Levitan and the admitted prior art had been discussed above. The admitted prior art further discloses that the processor is a network processor. (See pg. 1, line 5 and line 20).

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phung My Chung whose telephone number is 703-305-9686. The examiner can normally be reached on Monday to Friday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Albert Decady can be reached on 703-305-9595. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 872-9306 for regular communications and (703) 872-9306 for After Final communications.
Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-3900.

PHUNG M. CHUNG
PRIMARY EXAMINER